IN THE CLAIMS

1. (Original) A semiconductor memory structure comprising:

at least one adjacent pair of trench storage memory cells present in a Si-containing substrate, each memory cell including a vertical transistor overlaying a trench capacitor; strap outdiffusions present on each vertical sidewall of the trench storage memory cells, wherein said strap outdiffusions interconnect said vertical transistor and said trench capacitor of each memory cell to said Si-containing substrate; and

a punchthrough stop doping pocket located between each adjacent pair of trench storage memory cells, said punchthrough stop doping pocket is centered between said strap outdiffusions.

2. (Original) The semiconductor memory structure of Claim 1 wherein a plurality of adjacently paired trench storage memory cells are employed, and said punchthrough stop doping pockets are positioned at substantially the same location within the Si-containing substrate thereby eliminating alignment tolerance in the structure.

3. (Original) The semiconductor memory structure of Claim 1 wherein said trench capacitor comprises a buried plate diffusion region present about a storage trench, a node dielectric lining said storage trench and a N+ polysilicon layer present on said node dielectric.

4. (Original) The semiconductor memory structure of Claim 1 wherein said vertical transistor comprises a gate dielectric present on sidewalls of a storage trench and a N+ doped polysilicon gate conductor present on said gate dielectric.

5. (Original) The semiconductor memory structure of Claim 1 wherein said vertical transistor and said trench capacitor are separated by a trench top oxide layer.

6. (Original) The semiconductor memory structure of Claim 1 wherein said punchthrough doping pocket includes a P-type dopant.

7. (Original) The semiconductor memory structure of Claim 6 wherein said punchthrough doping pocket has a dopant concentration of about 1E18 cm^{-3} or less.

8. (Original) The semiconductor memory structure of Claim 1 further comprising wordlines present atop each trench storage memory cell.

9. (Original) The semiconductor memory structure of Claim 8 wherein said wordlines are in contact with said vertical transistors by means of a conductive plug.

10. (Original) The semiconductor memory structure of Claim 8 wherein said wordlines include a conductive material, a nitride cap present atop said conductive

material and nitride sidewall spacers present on exposed sidewalls of said conductive material and said nitride cap.

11. (Original) The semiconductor memory structure of Claim 8 further comprising bitline conductors formed atop said wordlines, said bitline conductors and said wordlines are isolated from each other.

12. (Original) A method for forming a semiconductor memory structure comprising the steps of:

(a) forming at least one adjacent pair of trench storage memory cells present in a Si-containing substrate, each memory cell including a vertical transistor overlaying a trench capacitor and strap outdiffusions present on each vertical sidewall of the trench storage memory cells, wherein said strap outdiffusions interconnect said vertical transistor and said trench capacitor of each memory cell to said Si-containing substrate; and

(b) forming a punchthrough stop doping pocket between each adjacent pair of trench storage memory cells, said punchthrough stop doping pocket is centered between said strap outdiffusions and self-aligned to said trench capacitors.

13. (Original) The method of Claim 12 wherein step (a) includes the steps of: forming oxide filled troughs atop said Si-containing substrate; forming a patterned photoresist atop said oxide filled troughs, said patterned photoresist having

openings that expose portions of an alternating pair of oxide filled troughs, while protecting the oxide filled tough next to said alternating pair; removing oxide from said portions of alternating pair of oxide filled troughs so as to expose a surface of said Si-containing substrate; and etching storage trenches into exposed surfaces of said Si-containing substrate.

14. (Original) The method of Claim 13 further comprising forming a buried plate diffusion region about said storage trenches; lining a portion of said trenches with a node dielectric; and filling a portion of said trenches with N+ polysilicon.

15. (Original) The method of Claim 14 further comprising removing a portion of said N+ polysilicon from said trenches to form a region of recessed N+ polysilicon; forming a strap outdiffusion region about a portion of said storage trenches; forming a top trench oxide on said recessed N+ polysilicon; forming a gate dielectric on each exposed sidewall of said storage trenches; and filling said trenches with additional N+ polysilicon thereby forming polysilicon lines.

16. (Original) The method of Claim 15 further comprising forming active area resist stripes orthogonal to said trench storage memory cells and forming isolation trench regions in regions not protected by said active area resist stripes.

17. (Original) The method of Claim 12 wherein step (b) includes an implant process which is performed in an opening adjacent to said pair of trench storage memory cells.

18. (Original) The method of Claim 17 wherein said opening includes sidewall spacers.

19. (Original) The method of Claim 12 further comprising forming wordlines above said trench memory cells after step (b) is performed.

20. (Original) The method of Claim 19 further comprising forming bitline conductors above said wordlines.